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Linear and Periodic State Integrated Circuits Noise Simulation Benchmarking

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***Abstract*—Advanced noise simulation is performed using linear and periodic state RF-CMOS circuit vehicles. As a linear vehicle, an operation amplifier is designed with two amplification stages while as periodic state, a ring oscillator operating in the high frequency region. The small signal noise analyses and phase noise analyses are benchmarked versus large signal direct time domain noise analysis, in relation to the obtained accuracy, the simulation parameters ruling the accuracy and the needed simulation time. The theoretical background of direct time domain (transient) noise analysis, its implementation and the used simulation model together with simulation time-saving and circuit diagnostics capabilities are addressed. In addition, the respective MOSFET noise sources – thermal, flicker and gate noise – are analyzed per device, versus their contribution and their simulation accuracy for both cases (linear and periodic state). Simulation guidelines for a proper noise behavior extraction are summarized and categorized according to each circuit type.**

***Index Terms*—cmos, transient noise, AC noise, PNOISE, linear circuit, periodic state circuit, simulation guidelines**

I. Introduction

Technology enabled high integration, high performance RF and mmWave applications and advanced System on Chip implementations [1]. The device noise significantly affects the overall performance, which is translated to data losses, weak signal processing and low signal to noise ratio (SNR) [2]. Depending on the targeted application, the noise sources that have a significant effect on the circuit vary. In this work, using SPECTRE simulator, noise simulation guidelines for two major circuit categories, linear and periodic state, are provided along with the dominant noise sources in a wide spectrum of applications.

The dominant noise sources that contribute the most in CMOS processed integrated circuits are thermal noise and flicker $(1/f)$ noise. Occasionally, a wider variety of noise sources are introduced such as shot noise, generation/recombination noise and "popcorn" noise [3]. The aforementioned noise sources, in the applications targeted by this paper, have a negligible contribution to the final noise and thus are not taken into consideration. In high frequency operating circuits in the RF and mmWave range, the gate induced noise is also considered with a significant contribution to the total noise of the circuit.

Thermal noise is generated by the random movement of electrons due to their thermal energy [4] - [7], and has a non-zero contribution to the total device noise regardless of the operating frequency. For MOS devices operating in saturation region the noise spectral density due to thermal fluctuation in the channel of a MOSFET can be expressed as [2], [8] - [9],

$$\frac{\overline{i_{th}^2}}{\Delta f} = \frac{8kTg_m}{3} \tag{1}$$

where i_{th} is the channel current due to thermal noise, k is the Boltzmann constant, T is the temperature and g_m is the device transconductance. Thermal noise is independent of the operating frequency of the circuit. The noise behavior described by the equation above, was confirmed though simulations with both direct time domain noise (also known as transient noise) and AC noise analysis. The power spectral density of both analyses is depicted in the Fig. 1a as to verifying the behavior and accuracy [2] of the transient noise and AC noise, respectively.

Contrary to the thermal noise, the flicker noise is inversely proportional to the operating frequency of the device and thus, for low frequency and audio applications, is dominant [10] - [11]. The flicker voltage noise behavior of a MOSFET device, is described according to the following formula [2], [8] - [9],

$$V_{flicker}^2(f) = \frac{K_f}{C_{ox}^2 \times W \times L \times f} \tag{2}$$

where C_{ox} is the gate capacitance per unit area, f is the operating frequency, W and L are the width and length of MOSFET's channel respectively and K_f is the flicker noise coefficient. The transient noise and AC noise analyses, for the flicker noise, are introduced in Fig. 1b. The results of the two simulations (transient and AC noise) are in great agreement and satisfactorily describe the flicker noise at a wide frequency spectrum.

RF/mmWave circuits targeted to 5G/6G applications [2], suffers from gate induced noise which have significant noise contribution. Thus, the low noise performance has a grave importance. For MOSFET devices at deep – nanometer scale, the gate oxide thickness has significantly shrunk. Hence, the coupling effect between gate and channel increased aggressively [12]. The gate induced noise current of the MOSFET corresponds to the thermal noise due to the appended conductance in parallel with the gate-source parasitic capacitance, according to the formula below [8], [13],

$$\frac{\overline{i_g^2}}{\Delta f} = \frac{16kT}{15g_m}\omega^2 C_{gs}^2 \tag{3}$$

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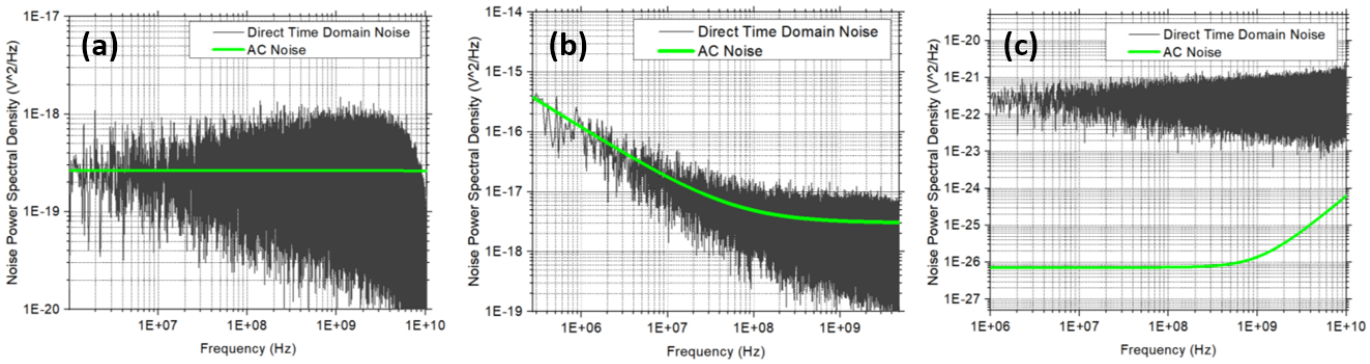

Fig. 1. MOSFET transient noise vs AC noise PSD analysis on a) thermal noise, b) flicker noise and c) gate induced noise.

where C_{gs} is the gate-source parasitic capacitance and ω is the frequency. For the standard device MOSFET models such as BSIM4 or even PSP [14] - [15], the gate induced noise, contrary to thermal and flicker noise, increases with frequency. The transient and AC noise analysis are not matched, as illustrated in Fig. 1c. These two noise simulations do not agree because of the restrictions in relation to the noise file of independent sources [2], [13]. To correct the gate induced noise behavior, an RC high pass filter must be introduced to the circuitry topology as to achieve the correct gate induced noise behavior [2].

II. CMOS Noise Simulation

The small signal approximation is used in commercial noise analysis and simulation tools, as to assess the noise contribution and interference on a circuit or device. The root assumptions for the circuit under test are either a stationary operating point that the circuit has, or a periodic steady state of interest. Furthermore, the noise contributions generated by devices must be small enough as not to alter the circuit's operating point or the periodic state of interest. Hence, noise analysis is converted to a linear problem which is easier to solve by means of the superposition principle [16].

In IC designs, there is a large-signal noise analysis problem that needs to be solved in the time domain and thus, transient noise analysis was introduced, whose behavior is similar to the traditional transient analysis. The key difference between these two time-domain analyses is that in transient noise analysis, there is an injection of random noise signals from all topology's noise sources at each time step of the analysis. This white noise signals generation in the time domain, can be approximated as [16] - [17],

$$n(t) = \sigma \times \eta(t, \Delta t) \tag{4}$$

where, $n(t)$ is a white noise signal with bandwidth F_{max} and $\eta(t, \Delta t)$ is a random number with Gaussian probability distribution. This random number is updated at each time step Δt of the analysis. The above variables, σ and Δt, that describes the white noise signal $n(t)$, are given below [17]:

$$\sigma = \sqrt{\overline{n^2} \times F_{max}} \quad , \quad \Delta t = \frac{1}{2 \times F_{max}} \tag{5}$$

The $\overline{n^2}$ coefficient is the noise power spectral density of an ideal noise source. At low operating frequencies, the noise spectral density matches the ideal noise PSD but at frequencies comparable to F_{max}, the deviation of the noise PSD is significant [16].

In addition to transient noise analysis, the AC noise analysis was introduced. The AC noise analysis consists of an AC analysis and a noise analysis as to calculate the output noise and equivalent input noise in a circuit. The RMS sum in the circuit, at a specific node, is the output noise of the AC analysis [18]. The AC noise analysis, in contrast to the transient noise, is simulated in the frequency domain by linearizing the circuit equations around it's operating point. The noise sources of the circuit are frequency dependent since at AC circuits, frequency is the sweep variable. To generate a frequency dependent noise signal in time domain, the extension of white noise signal approach is performed, by the approximation of the frequency dependency using a set of step functions [16]. The frequency range of interest is divided in several steps from F_{min} to F_{max}. Dividing this frequency range into N steps, the frequency step mapping derives from the following formula,

$$f_i = \frac{F_{max}}{2^i} \quad , \quad i = 0, 1, ..., N \tag{6}$$

where $f_0 = F_{max}$ and $f_N = F_{min}$. The white noise sources are created for each frequency step and thus, the total noise is the sum of all noise sources corresponding to the individual frequency step, as described by the following formula,

$$n(t) = \sum_{i=0}^{N} \sigma_i \times \eta\left(t, \frac{1}{2f_i}\right) \tag{7}$$

$$\sigma_i = \sqrt{\left(\overline{n^2}(f_i) - \overline{n^2}(f_{i-1})\right) \times 2f_i} \tag{8}$$

For the amplitude of noise sources to match the frequency dependent noise spectral density, its calculation is given by (8) above [16] - [17].

III. Noise Simulation Vehicles

From a simulation point of view, there are two basic noise simulations performed to extract noise contribution, the AC

Noise and the PNOISE analysis. Both simulations, describe the noise properties in the frequency domain by linearizing the circuit equations around either it's operating point for linear circuits like an operational amplifier, or the periodic state of interest for periodic circuits like oscillators, for AC noise and PNOISE analysis, respectively [2], [16]. Depending on the circuit of interest, AC noise analysis for linear circuit topologies (Operational Amplifiers, LNAs, Filters, etc.), or PNOISE analysis for periodic state circuit topologies (VCOs, DCOs, Ring Oscillators, etc.) are performed as to extract the noise behavior of the vehicle under test. In this paper, as a linear vehicle, a custom opamp circuit topology is designed and as a periodic state vehicle, a ring oscillator is designed and additionally, AC noise and PNOISE analyses are performed in the respective topologies. Both vehicles were designed 1.2V 65nm RFCMOS process.

A. Linear Circuits Noise Simulation

A two stage operational amplifier is designed using noiseless resistor loads and noiseless current sources. The only devices that contribute to the total noise of the topology is the n-channel and p-channel CMOS transistors at the differential pair and the output stage as to identify and evaluate only the CMOS noise sources . The circuit topology is depicted in the Fig. 2. The opamp open loop gain and bandwidth are 25.4 dB and 840 MHz, respectively. At the IN+ terminal of the opamp, a sine voltage source of f = 50 kHz, V_{ampl} = 1 mV and a DC offset of 600 mV was connected. At the IN- terminal of the opamp, a DC voltage source of 600 mV was connected.

Since the opamp vehicle is a linear circuit, the noise analyses that can be supported and executed are the transient noise and the AC noise. The simulation results of both transient noise and AC noise analysis are depicted in Fig. 3. The proper simulations setups are presented in Table I.

Due to the fact that the bandwidth of the designed opamp is limited to 840 MHz, the noise F_{max} parameter should not exceed this value since at frequencies higher than the opamp's BW, the noise will be suppressed by the circuit itself. In this specific simulation, the noise F_{max} parameter was selected as

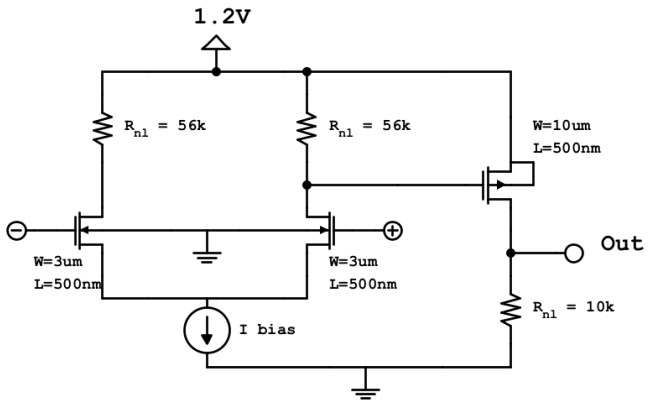

Fig. 2. Two stage opamp topology.

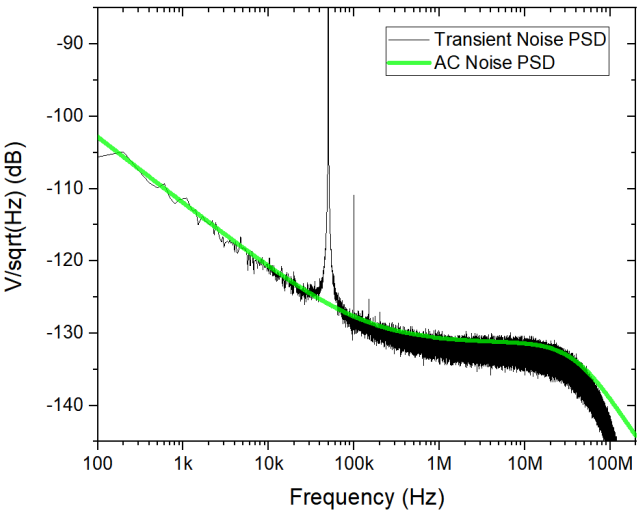

Fig. 3. AC noise vs transient noise performance of opamp vehicle.

to have a good enough accuracy and at the same time, to have a reasonably simulation time.

With the increase of the noise F_{max} parameter, the time step of pseudo-random noise sources adding to the circuit decreases and thus, the simulation time increases. Similarly, the noise F_{min} parameter defines the lowest frequency of interest and at frequencies below the noise F_{min} parameter, the noise behavior of the circuit is simulated as flat. The simulation results of AC noise matched to a large extent to the simulation results derived from transient noise analysis while both analyses follow the same spectral behavior. However, the major benefit of AC noise over transient noise analysis is that the simulation time of AC noise is much shorter than transient noise one.

TABLE I
OPAMP TRANSIENT NOISE VS AC NOISE SIMULATION SETUP.

Transient Noise Analysis		**AC Noise Analysis**	
Noise F_{max}	200 MHz	Sweep var.	Frequency
Noise F_{min}	100 Hz	Range	100 Hz - 200 MHz
Noise seed	1111	Type	Log.
Fund.Freq.	50 kHz	Pts/Dec.	10000
PSD F_{max}	200 MHz	Out noise +	/Vout
PSD F_{min}	100 Hz	Out noise −	/gnd!
Samples	127744000	Inp. noise	/Vsource
Window Size	3992000	-	-
CPU time	62 min, 13 sec	CPU time	2 sec

The overall noise contribution for each opamp stage, is depicted in the Fig. 4. The main noise sources that contribute to the total circuit noise are thermal and flicker noise. Flicker noise has a significant noise contribution at low operating frequencies while on the contrary, thermal noise has a significant noise contribution at higher operating frequencies. Furthermore, the opamp differential pair has the main noise contribution to the overall circuit.

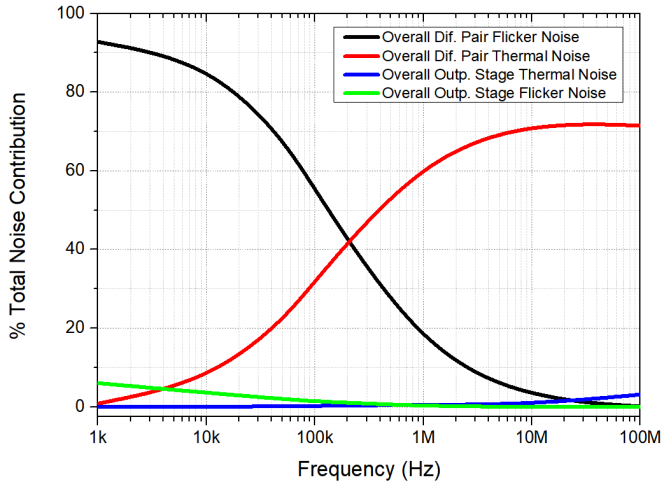

Fig. 4. Overall noise contribution data per stage in opamp circuit topology.

B. Periodic State Circuits Noise Simulation

As a periodic state vehicle, two ring oscillator topologies with different MOSFET devices are designed. The devices used for implementing these two topologies are, the native CMOS devices and the RF CMOS devices, respectively. The main difference between these two types, in model level and schematic simulation performance, is that the native devices are modeled with a standard BSIM4V4 compact model, while RF macro models with respective subcircuit are available for the RF FETs. As a result, in the RF model, the gate network impedance of the FET is taken into consideration. Thus, the RF CMOS devices, at high operating frequencies, have a significant gate induced noise contribution to the total noise of the topology. In contrariety, the native devices have only flicker and thermal noise contribution as well as noise from current leakages of the device itself. The circuit topology of the ring oscillator is depicted in Fig. 5 together with the design parameters for both circuit implementations.

For the noise analysis of a periodic state circuit, such as the ring oscillator, two analyses must be performed as to derive a complete noise behavior of the topology. A PNOISE in combination with a PSS (Periodic Steady State) analysis are performed and the simulation results are compared with the results from the transient noise analysis. A comparison between these noise analyses of both circuit versions, are depicted in Fig. 6. The transient noise and PNOISE results are matched to a large extend for both implementations while the simulation time of transient noise is way longer than PNOISE's. Increasing the points/decade of the PNOISE analysis, a better harmonics amplitude match achieved, as illustrated in Fig. 6c.

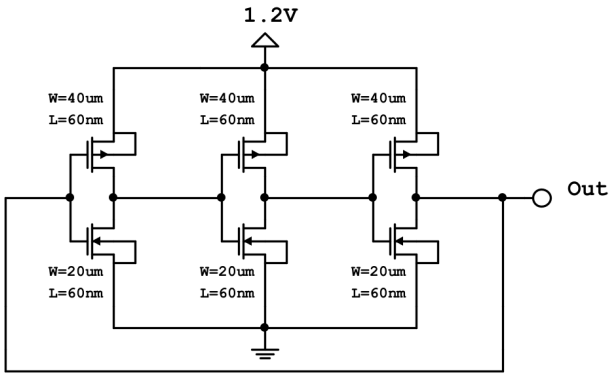

Fig. 5. Ring oscillator topology.

The fundamental oscillation frequency of the ring oscillator depicted in Fig. 5, is 40.5 GHz for the native device implementation and 25 GHz for the RF device implementation. Due to the fact that the RF device model takes into consideration the MOSFET gate impedance network, the oscillation frequency is degraded relative to the oscillation frequency of the native device implementation. The transient noise and PNOISE simulations setup for the native as well as for the RF device implementation, are presented in Table II below.

TABLE II
RING OSCILLATOR TRANSIENT NOISE AND PNOISE SIMULATION SETUP FOR BOTH IMPLEMENTATIONS.

Transient Noise Analysis		**PNOISE Analysis**	
Noise F_{max}	2 THz	Sweep type	absolute
Noise F_{min}	100 MHz	Range	100 MHz - 2 THz
Noise seed	1111	Type	Logarithmic
PSD F_{max}	2 THz	Pts/Dec.	10000
PSD F_{min}	100 MHz	Out noise +	/Out
Samples	163184640	Out noise −	/gnd!
Window Size	39942000	Noise type	timeaverage
CPU time (native model)	85 min, 3 sec	CPU time (native model)	1 min, 37 sec
CPU time (RF model)	166 min, 5 sec	CPU time (RF model)	2 min, 45 sec

The beat frequency of the PSS analysis that performed along with the PNOISE analysis, is chosen accordingly to the oscillation frequency of the ring oscillator. The PSS analysis calculates the exact oscillation frequency even if the beat frequency is not estimated correctly.

The spot noise contribution must be calculated only at the oscillation frequency of the ring oscillator. Performing a channel length sweep, different oscillation frequencies occurred. The relation between the channel length of the MOSFETs and the oscillation frequency of both implementations is inversely proportional meaning that with the increase of the channel length, the oscillation frequency decreases. Hence, the overall noise contribution is calculated for a relatively wide oscillation frequency range as to derive the gate induced noise contribution trend.

As expected, gate induced noise contribution is decreasing with frequency because at high oscillation frequencies, noise from devices' current leakages are also introduced. Thus, the percentage of the total gate noise contribution must decreasing with frequency considered that the gate noise behavior is modeled relatively flat regardless of the oscillation frequency.

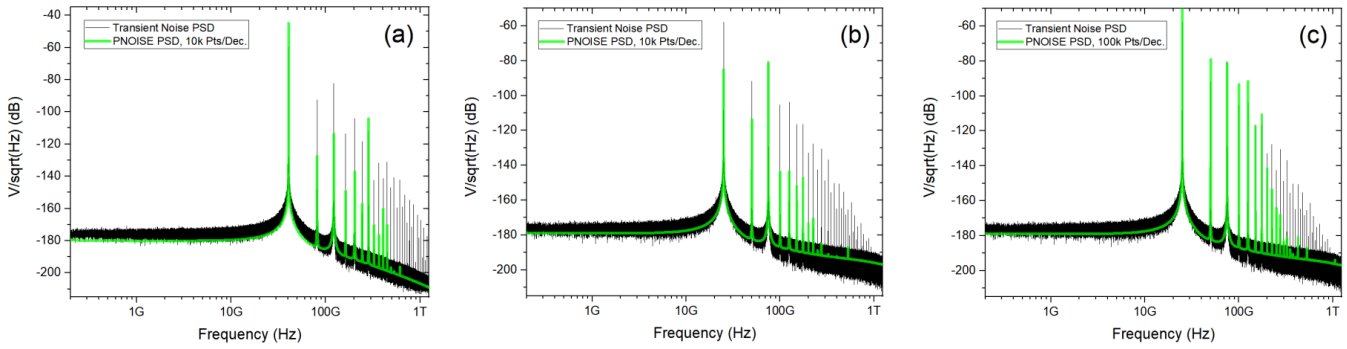

Fig. 6. Transient noise vs PNOISE performance of the ring oscillator with a) native CMOS devices, b) RF CMOS devices using 10k points/decade and c) RF CMOS devices using 100k points/decade.

Having (3) as reference, gate induced noise must increases with frequency and thus, for high operating frequencies, gate induced noise must be dominant. The gate induced noise performance trend, illustrated at Fig. 7, is not accurate noise performance as also described in [2]. Flicker noise at the frequency range of the designed ring oscillator is negligible.

Some basic metrics in ring oscillators or any kind of oscillator circuitry are period jitter and eye diagram. These metrics can only be estimated by transient noise analysis. Considering the results depicted in Fig. 8, native compact FET models are not suitable for high frequency applications and only RF models should be used because gate impedance network is taken into consideration.

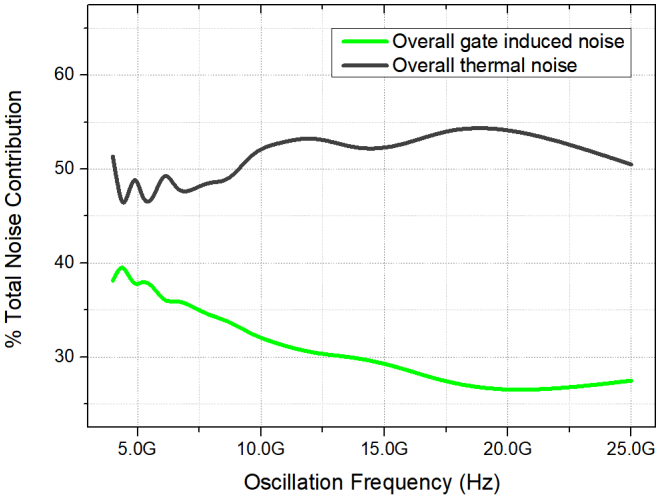

Fig. 7. Overall gate induced noise and thermal noise contributions of the ring oscillator implemented with RF model devices.

IV. Noise Simulation Guidelines

Linear and periodic circuit topologies indicate a specific range of noise analyses that can be supported and executed. Simulation guidelines, restrictions and performance for noise analysis depending on the circuit type are provided in Table III. The presented noise simulation guidelines are, for the most part, generic and can be applied in any type of circuitry as

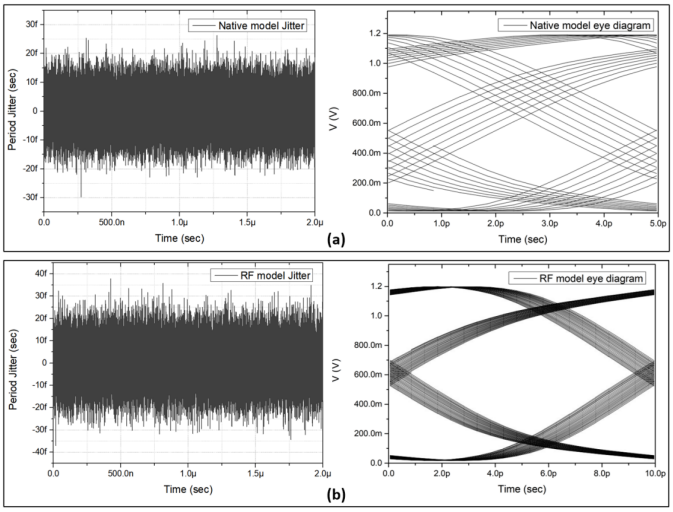

Fig. 8. Ring oscillator period jitter and eye diagram using a) standard BSIM4V4 compact models, b) RF macro models, respectively.

long as the circuit falls under one of the two circuit categories analyzed by this work (linear or periodic state). Furthermore, the simulation guidelines are independent of the technology used but the results may differ to a large extend if an alternative process, besides 1.2V 65nm RFCMOS, is used.

Linear circuits can be accurately simulated noise wise with AC noise, with optimum simulation times and therefore the need of transient noise analysis arises only when really low AC signals and low DC signals impose operation close to the noise floor of the circuit. In all other cases, AC noise is sufficient accuracy wise and optimum simulation time wise as to be used for the noise performance verification.

On the other hand, in periodic state typologies, PNOISE can be efficiently used for derivation of circuit noise performance if the device models are accurate and suitable for the specified application. However, misleading results may appear when higher harmonics noise performance needs to be captured. PNOISE analysis is efficient time wise and accurate results, concerning the noise performance of higher harmonics, can be achieved with low impact on simulation time. Hence, in periodic state circuits, when it comes to rapid and accurate

TABLE III
NOISE SIMULATION GUIDELINES FOR LINEAR AND PERIODIC STATE TOPOLOGIES.

Circuit Type	**Linear Circuit**		**Periodic State Circuit**		
Circuit Vehicles	OpAmps, Filters, LNAs, DC biased circuitries		VCOs, DCOs, Mixers, Dividers		
Frequency Operation Region	Baseband		RF and mmWave		
Device Model	standard BSIM4V4		standard BSIM4V4 + RF macro model		
Noise Analysis Type	Transient noise AC noise PNOISE + PSS	✓ ✓ ✗	Transient noise AC noise PNOISE + PSS		✓ ✗ ✓
Noise Simulation Time	Faster execution:	AC noise	Faster execution:		PNOISE
Simulation Accuracy	Transient noise accuracy:	Satisfactorily	Transient noise accuracy:	**BSIM4V4:** **RF model:**	Bad → No gate resistance Poor → Gate resistance considered but incorrect noise behavior.
	AC noise accuracy:	Satisfactorily	PNOISE accuracy:	**BSIM4V4:** **RF model:**	Bad → No gate resistance, harmonic noise amplitudes do not match. Good → Gate resistance considered but incorrect noise behavior. Better harmonic noise amplitude match.
Parameters that Increases Simulation Accuracy	Transient noise:	Fmax ↑ → Time Step ↓ Number of Samples ↑ (simulation time increases)	Transient noise:		Fmax ↑ → Time Step ↓ Number of Samples ↑ (simulation time increases)
	AC noise:	Points/Decade↑ (simulation time increases)	PNOISE:		Points/Decade↑ (simulation time increases)
Recommented Noise analysis	AC noise Transient noise:	✓ ✗	Transient noise PNOISE	**BSIM4V4:** **RF model:** **BSIM4V4:** **RF model:**	✗ ✓ ✗ ✓ ✓
Dominant Noise Sources	Low frequencies: High frequencies:	Flicker noise Thermal noise	Low frequencies: High frequencies:		Thermal noise Gate induced noise

circuit noise extraction, PNOISE analysis is preferred because the execution is way faster than performing a transient noise analysis.

V. CONCLUSION

The basic noise sources that significantly contribute to the total circuit noise were extensively addressed. Noise simulation accuracy using native and RF models is examined and simulation time of each analysis that was performed also provided. Gate induced noise performance trend as well as the impact of it to the simulations results was obtained. Additionally, basic metrics that describe the circuit behavior and functionality but can only be provided by transient simulation, were illustrated. Noise simulation guidelines depending on the type of the designed circuit and its bandwidth, the device models, the simulation time and accuracy and the constraints for higher harmonics noise performance capture, were provided. Within them, simulation parameters that increases the accuracy along with the dominant noise sources at specific frequency ranges were also addressed. Detailed noise simulation guidelines depending on the targeted circuit type and its operating frequency were provided for faster and more accurate circuit noise performance extraction.

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